UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,372	11/21/2001	Richard H. Lane	M4065.0338/P338-A	1348

45374 7590 12/24/2008

DICKSTEIN SHAPIRO LLP
1825 EYE STREET, NW
WASHINGTON, DC 20006

EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
12/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/989,372	LANE, RICHARD H.	
	Examiner	Art Unit	
	Chuong A. Luu	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-32,34-39,41,44-47,49,51-59 and 65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *59 and 65* is/are allowed.

6)☒ Claim(s) *29-32,34-39,41,44-47,49 and 51-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 29-32, 34-39, 41, 44-47, 49, 51-59 and 65 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The Rejections

Claims 55-56 are rejected under 35 U.S.C. 102(e) as being anticipated by Fazan et al. (U.S. 5,392,189)

Fazan discloses a capacitor device with

(55) a lower electrode (85) provided fully within a first insulating layer (83), said lower electrode (85) comprising an electropolished patterned metal layer (85) having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom;

a second insulating layer (87) provided over said electropolished patterned metal layer (85) and in contact with said first insulating layer (83);

an upper electrode (88) provided over said second insulating layer (87) (see Figure 14B);

(56) wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides (see column 7, lines 7-15).

Regarding the process limitations recited in claim 55 (an electropolished patterned metal layer is electropolished down...), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 29-32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng et al. (U.S. 6,184,081) in view of Fazan et al. (U.S. 5,392,189).

Jeng discloses a DRAM structure with

(29) a substrate (1);

an insulating layer (16) provided over said substrate (1);

an electropolished patterned metal layer (20) provided within an opening (18a) of said insulating layer (16), wherein said electropolished metal layer (20) and wherein a top surface of said electropolished metal layer (20) is electropolished down to said insulating layer (16) so that said top surface of said electropolished metal layer (20) is at the same level with a top surface of said insulating layer (16) (see Figures 2-5);

a photoresist plug (21a) provided within said opening (18a) and over and in contact with said electropolished patterned metal layer (20) (see Figures 2-5).

Jeng teaches the above outlined features except to disclose the specific thickness and materials of the metal layer. However, Fazan discloses a capacitor device with **(30)** wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides (see column 7, lines 7-15); **(31)** wherein said electropolished patterned metal layer contains a noble metal (see column 7, lines 7-15); **(32)** wherein said electropolished patterned metal layer is a platinum layer (see column 7, lines 7-15); **(35)** wherein said electropolished patterned metal layer forms a lower capacitor

electrode of said semiconductor device (see Figure 14B). Even through, Jeng and Fazan do not explicitly disclose the thicknesses of the metal layer approximately 50-300Å. However, the thicknesses of the metal layer approximately 50-300Å is considered to be obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Jeng and Fazan to select the specific thickness and materials for the metal layer, since it has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. . In re Leshin, 125 USPQ 416 and In re Aller, 105 USPQ 233 (see MPEP 2144.05). Additionally, since Jeng and Fazan are both from the same field of endeavor (semiconductors), the purpose disclosed by Fazan would have been recognized in the pertinent art of Jeng.

Regarding the process limitations recited in claim 29 (an electropolished patterned metal layer is electropolished down...), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Claims 36-39, 41, 44-47, 49 and 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan et al. (U.S. 5,392,189) in view of Taniguchi (U.S. 6,559,494).

Fazan discloses a capacitor device with

(36) a transistor including a gate fabricated on a semiconductor substrate (7) and including a source/drain region (30) in said semiconductor substrate (7) disposed adjacent to said gate;

an insulating layer (83) provided over said substrate (7); and a container capacitor including a lower electrode (85), a dielectric layer (87) over said lower electrode (85), and an upper electrode (88) over said dielectric layer (87), and said lower electrode (85) having a surface aligned over said source/drain region (30), wherein said lower electrode (85) comprises an electropolished patterned metal layer which is situated fully within said insulating layer (83), wherein said electropolished patterned metal layer (85), and wherein said dielectric layer (87) is in contact with said insulating layer (83) (see Figure 14B);

(37); (45) wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides (see column 7, lines 7-15);

(38); (46) wherein said electropolished patterned metal layer contains a noble metal (see column 7, lines 7-15);

(39); (47) wherein said electropolished patterned metal layer is a platinum layer (see column 7, lines 7-15);

(44) a processor (transistor);

an integrated circuit (plug) coupled to said processor (transistor), at least one of said integrated circuit and said processor comprising a container capacitor provided within an insulating layer (83), said container capacitor including a lower electrode (85) and an upper electrode (88), said lower electrode (85) comprising an electropolished patterned metal layer (85), wherein a top surface of said electropolished patterned metal layer (85) is at the same level with a top surface of said insulating layer (83) such that said lower electrode (85) does not extend above the top surface of said insulating layer (83), and said upper electrode (88) (see Figure 14B);

(51) wherein said integrated circuit is a memory module (see Figure 14B);

(52) wherein said memory module is a DRAM memory (see column 4, lines 32-33);

Fazan teaches everything above except for utilizing a doped polysilicon material for the upper electrode. However, Taniguchi discloses a semiconductor device with **(36); (44)....** said upper electrode comprising doped polysilicon (see column 3, lines 38-48).

Even through, Fazan and Taniguchi do not explicitly disclose the thicknesses of the metal layer approximately 50-300Å. However, the thicknesses of the metal layer approximately 50-300Å is considered to be obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to

modify the teaching of Fazan (accordance with the teaching of Taniguchi) to employ the specific thickness and materials for the metal layer, since it has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. . In re Leshin, 125 USPQ 416 and In re Aller, 105 USPQ 233 (see MPEP 2144.05). Additionally, since Fazan and Taniguchi are both from the same field of endeavor (semiconductors), the purpose disclosed by Taniguchi would have been recognized in the pertinent art of Fazan.

Regarding the process limitations recited in claims 36 and 44 (an electropolished patterned metal layer is electropolished down...), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Claims 53-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan et al. (U.S. 5,392,189) in view of Taniguchi (U.S. 6,559,494) and further in view of Hashimoto (U.S. 6,515,370).

Fazan and Taniguchi disclose everything above except for fabricating specific memory device like SRAM and MCM. Furthermore, Romankiw discloses an integrated

circuit with **(53)** wherein said memory module is a SRAM memory (see column 6, lines 55-56); **(54)** wherein said memory module is a MCM memory (see column 8, lines 20-23). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Fazan and Taniguchi (accordance with the teaching of Hashimoto) to fabricate the specific semiconductor device on the basis of its suitability for the intended use as a matter of obvious design choice involves only routine skill in the art. Additionally, since Fazan, Taniguchi and Hashimoto are from the same field of endeavor (semiconductors), the purpose disclosed by Hashimoto would have been recognized in the pertinent art of Fazan and Taniguchi.

Claims 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan et al. (U.S. 5,392,189).

Fazan teaches every thing above except for explicitly disclose the thicknesses of the metal layer approximately 50-300Å. However, the thicknesses of the metal layer approximately 50-300Å is considered to be obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching Fazan since it has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP 2144.05).

Allowable Subject Matter

Claims 59 and 65 are allowed.

The following is an examiner's statement of reasons for allowance: The examiner has reviewed the prior art in light of applicant's claimed invention and finds that the combined claims define over the prior art. The cited prior art does not disclose or suggest a semiconductor device inter alia the limitations "…a barrier conductive layer provided within the contact opening, the barrier conductive layer being disposed along a bottom and sidewalls of the contact opening, wherein the barrier conductive layer has a first thickness and wherein a length of upwardly extending portions of the barrier conductive layer that are disposed along the sidewalls of the contact opening is equal to the first height; a lower platinum electrode provided over the barrier conductive layer, the lower platinum electrode being disposed along a bottom portion and sidewall portions of the barrier conductive layer, wherein a length of upwardly extending portions of the lower platinum electrode that are disposed along the sidewall portions of the barrier conductive layer is equal to the first height minus the first thickness; a dielectric layer provided over the lower platinum electrode, the dielectric layer being disposed along a bottom portion and sidewall portions of the lower platinum electrode and on an upper surface of the barrier conductive layer. . …."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong A Luu/
Primary Examiner, Art Unit 2892
December 19, 2008